REMARKS

In the Office Action, the Examiner noted that claims 1, 3-6, 8-14, 16, and 18-23 are pending in the application. The Examiner rejected claims 1, 3-6, 8-14, 16, and 19-23. Claim 18 is objected to, but indicated as allowable. In view of the above amendments and the following discussion, the Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicants believe that all of these claims are now in condition for allowance.

I. Rejection Of Claims Under 35 U.S.C. §102

The Examiner rejected claims 10-11 as being unpatentable over Mahajan (United States patent 6,618,358, issued September 9, 2003). The Applicants respectfully traverse the rejection.

The Applicants submit that Mahajan does not disclose or suggest at least "a programmable fabric portion comprising a plurality of clock based functionalities, wherein each of the clock based functionalities performs processing on the high data rate input data stream in accordance with a clock chosen from among the plurality of recovered clocks and a reference clock," as recited in claim 10.

Mahajan teaches a method and apparatus for switching a clock source from among multiple T1/E1 lines. More specifically, Mahajan teaches a network access server (NAC) that recovers clock signals from incoming T1/E1 lines. A demultiplexor in the NAC selects and outputs one of the recovered clock signals, which is then used to drive the internal data bus of the NAC as a reference clock. The demultiplexor may also select a free running clock signal from an oscillator as its output.

The Applicants note that Mahajan does not disclose that the free running clock signal is a reference clock signal. At best, Mahajan discloses that the free running clock signal is provided as an input to a demultiplexor whose output is a reference clock signal. However, at the point at which the demultiplexor makes its selection, no reference clock signal yet exists. Thus, the demultiplexor cannot select from among a plurality of recovered clocks and a reference clock, as do the clock based functionalities recited in claim 10.

Since Mahajan, fails to teach or suggest at least "a programmable fabric portion comprising a plurality of clock based functionalities, wherein each of the clock based functionalities performs processing on the high data rate input data stream in accordance with a clock chosen from among the plurality of recovered clocks and a reference clock," Mahajan does not teach or suggest each and every element of the Applicants' independent claim 10. Accordingly, the Applicants contend that independent claim 10 is not anticipated by Mahajan and, as such, fully satisfies the requirements of 35 U.S.C. §102.

Furthermore, claim 11 depends from claim 10 and recites at least all of the features recited in claim 10. Since Mahajan in does not teach or suggest every feature recited in independent claim 10, dependent claim 11 is also patentable and is allowable. Therefore, the Applicants contend that claims 10-11 are not anticipated by Mahajan and, as such, fully satisfy the requirements of 35 U.S.C. §102.

II. Rejection Of Claims Under 35 U.S.C. §103

A. Claims 1, 4-6, and 19-22

The Examiner rejected claims 1, 4-6, and 19-22 as being unpatentable over Mahajan (United States patent 6,618,358, issued September 9, 2003) in view of Peace (United States patent 6,687,260, issued February 3, 2004) and further in view of Mindspeed ("T1/E1 Framer and Line Interface Bt8379"). The Applicants respectfully traverse the rejection.

As discussed above, Mahajan does not disclose or suggest at least "wherein each of the plurality of clock based functionalities performs processing of one of the first serial data and the second serial data in accordance with a clock chosen from among the first recovered clock, the second recovered clock and the reference clock," as recited in claim 1. In addition, for reasons similar to those provided above with respect to claim 1, Applicants submit that independent claims 6, 19, and 22 are patentable over Mahajan. As discussed in greater detail below, Peace and Mindpseed fail to bridge this gap in the teachings of Mahajan.

The Examiner acknowledges in the Office Action that "Mahajan et al. do not expressly teach: serial data; a plurality of clock based functionalities; each of the

plurality of clock based functionalities performs processing of one of the first serial data and the second serial data in accordance with a clock chosen from among the first recovered clock, the second recovered clock, and the reference clock" (Office Action, Page 6). The Examiner submits, however, that "Peace discloses: serial data" (Office Action, Page 6) and that "Mindspeed discloses: a plurality of clock based functionalities" (Office Action, page 6), and that these features, in combination with Mahajan, render the Applicants' claims obvious. The Applicants respectfully disagree.

Peace teaches an apparatus and method for flow control of non-isochronous data. One component of this apparatus is an I/O processor that "suitably converts the multi-bit data [of incoming signals] into a serial format and provides the serial data to [a] channel processor" (See Peace, column 4, lines 54-56).

Peace, however, does not teach each and every element of Applicants' independent claims 1, 6, 19, and 22. Namely, Peace, like Mahajan, does not teach or suggest processing serial data in accordance with a clock chosen from among a plurality of recovered clocks and the reference clock. In contrast, the I/O processor taught by Peace, which the Examiner appears to equate with the claimed "clock based functionality," merely processes serial data but does not select a clock from among recovered clocks for use in the processing. Peace does not even describe or illustrate a component for selecting a clock.

Mindspeed teaches a framer and line interface for T1/E1 and Integrated Service Digital Network (ISDN) primary rate interfaces. The framer and line interface combines a framer and transmit/receive slip buffers with an on-chip short/long-haul physical line interface.

Mindspeed, however, does not teach each and every element of Applicants' independent claims 1, 6, 19, and 22. Namely, Minspeed, like Peace and Mahajan, does not teach or suggest processing serial data in accordance with a clock chosen from among a plurality of recovered clocks and the reference clock. In contrast, Minspeed teaches a clock rate adapter but does not describe the adapter in detail.

Peace and Mindspeed thus fail to bridge the gaps in the teachings of Mahajan. Since none of Mahajan, Peace, and Hashiguchi teaches or suggests a component (*e.g.*, a clock based functionality of a logic fabric) that processes serial data from a

serial bit stream in accordance with a clock selected from among a plurality of clocks including recovered clocks and a reference clock, Mahajan in view of Peace and further in view of Mindspeed does not teach or suggest each and every element of the Applicants' independent claims 1, 6, 19, and 22.

In addition, the Applicants submit that none of Mahajan, Peace, and Mindspeed teaches or suggests at least a transceiver that comprises a plurality of clock based functionalities, each of which chooses a clock for processing of serial data, as recited in claims 1 and 6.

As discussed above, the Examiner acknowledges that Mahajan does not disclose a plurality of clock based functionalities. The Examiner submits, however, that this feature is taught by Mindspeed. The Applicants respectfully disagree.

By contrast, Mindspeed at best teaches a plurality of transceivers. Mindspeed does not teach, however, that each of these transceivers in turn comprises a plurality of clock based functionalities, nor that each of these clock based functionalities in each transceiver can select a clock for its functionality. As discussed in the Applicants' Specification at least in paragraph [0052], a transceiver includes a plurality (*e.g.*, at least three) clock based functionalities. "Each functionality selects a clock for its functionality and thus may operate according to different clocks in relation to each other." Mindspeed simply does not teach this feature, as recited in claims 1 and 6. Thus, the Applicants contend that claims 1 and 6 are allowable for these additional reasons.

Accordingly, the Applicants contend that independent claims 1, 6, and 19 are patentable over the combination of Mahajan, Peace, and Mindspeed and, as such, fully satisfy the requirements of 35 U.S.C. §103. Furthermore, claims 4-5 and 20-21 depend from claims 1 and 19, respectively, and recite additional features. Since Mahajan in view of Peace and further in view of Mindspeed does not teach or suggest Applicants' invention as recited in independent claims 1 and 19, dependent claims 4-5 and 20-21 are also patentable and are allowable. Therefore, the Applicants contend that claims 1, 4-6, and 19-22 are patentable over Mahajan in view of Peace and further in view of Mindspeed and, as such, fully satisfy the requirements of 35 U.S.C. §103.

B. Claim 3

The Examiner rejected claim 3 as being unpatentable over Mahajan in view of Peace and Mindspeed and further in view of Tang (US Publication No. 2002/0075981). The Applicants respectfully traverse the rejection.

As discussed above, Mahajan in view of Peace and further in view of Mindspeed does not teach or suggest Applicants' invention where a component selects a clock for processing of serial data from among a plurality of clocks including recovered clocks and a reference clock to use for the processing of the serial data, as recited by claim 1. This deficiency is not bridged by the teaching of Tang.

Therefore, Applicants contend that dependent claim 3 which depends from independent claim 1 and recites at least the same features, is patentable over the combination of Mahajan, Peace, Mindspeed, and Tang and, as such, fully satisfies the requirements of 35 U.S.C. §103.

C. Claims 8-9

The Examiner rejected claims 8-9 as being unpatentable over Mahajan in view of Peace and further in view of Ohtsuka (United States patent 5,388,100, issued February 7, 1995). The Applicants respectfully traverse the rejection.

As discussed above, Mahajan and Peace both fail to teach or suggest Applicants' invention where a component selects a clock for processing of serial data from among a plurality of clocks including recovered clocks and a reference clock to use for the processing of the serial data, as recited in the Applicants' independent claim 8. This deficiency is not bridged by the teaching of Ohtsuka.

Furthermore, claim 9 depends from independent claim 8 and recites additional features. Since Mahajan in view of Peace and further in view of Ohtsuka does not teach or suggest Applicants' invention as recited in independent claim 8, dependent claim 9 is also patentable and is allowable. Therefore, the Applicants contend that claims 8-9 are patentable over Mahajan in view of Peace and further in view of Ohtsuka and, as such, fully satisfy the requirements of 35 U.S.C. §103.

D. Claim 12

The Examiner rejected claim 12 as being unpatentable over Mahajan in view of Galuszka (US Patent No. 5,519,693, issued May 21, 1996). The Applicants respectfully traverse the rejection.

As discussed above, Mahajan does not teach or suggest Applicants' invention where a component selects a clock for processing of serial data from among a plurality of clocks including recovered clocks and a reference clock to use for the processing of the serial data, as recited by claim 10. This deficiency is not bridged by the teaching of Galuszka.

Therefore, Applicants contend that dependent claim 12 which depends from independent claim 10 and recites at least the same features, is patentable over the combination of Mahajan and Galuszka and, as such, fully satisfies the requirements of 35 U.S.C. §103.

E. Claim 13

The Examiner rejected claim 13 as being unpatentable over Mahajan in view of Peace. The Applicants respectfully traverse the rejection.

As discussed above, Mahajan and Peace fail to teach or suggest Applicants' invention where a component selects a clock for processing of serial data from among a plurality of clocks including recovered clocks and a reference clock to use for the processing of the serial data, as recited in the Applicants' independent claim 10.

Therefore, Applicants contend that dependent claim 13 which depends from independent claim 10 and recites at least the same features, is patentable over the combination of Mahajan and Peace and, as such, fully satisfies the requirements of 35 U.S.C. §103.

F. Claims 14 and 16

The Examiner rejected claims 14 and 16 as being unpatentable over Mahajan in view of Mann (United States patent 5,251,210, issued October 5, 1993). The Applicants respectfully traverse the rejection.

As discussed above, Mahajan fails to teach or suggest Applicants' invention where a component selects a clock for processing of serial data from among a plurality of clocks including recovered clocks and a reference clock to use for the processing of the serial data, as recited in the Applicants' independent claim 14. This deficiency is not bridged by the teaching of Mann.

Furthermore, claim 16 depends from independent claim 14 and recites at least the same features. Since Mahajan in view of Mann does not teach or suggest Applicants' invention as recited in independent claim 14, dependent claim 16 is also patentable and is allowable. Therefore, the Applicants contend that claims 14 and 16 are patentable over Mahajan in view of Mann and, as such, fully satisfy the requirements of 35 U.S.C. §103.

G. Claim 23

The Examiner rejected claim 23 as being unpatentable over Mahajan in view of Hashiguchi. The Applicants respectfully traverse the rejection.

As discussed above, neither Mahajan nor Hashiguchi teaches or suggests Applicants' invention where a component selects a clock for processing of serial data from among a plurality of clocks including recovered clocks and a reference clock to use for the processing of the serial data, as claimed in the Applicants' independent claim 23.

Hashiguchi fails to bridge this gap in the teachings of Mahajan. Hashiguchi teaches a system having a clock signal generating circuit for selectively generating requested clock signals. One component of this system is an output clock selector "for selectively supplying serial clock signals from [a] serial clock generator to a plurality of transmission circuits and a plurality of reception units" (See Hashiguchi, column 6, lines 55-58).

Hashiguchi, however, does not teach each and every element of Applicants' independent claim 23. Namely, Hashiguchi, like Mahajan, does not disclose that a reference clock is one of the clock signals from among which the output clock selector may choose. By contrast, Hashiguchi only teaches that the serial clock signals generated by the serial clock generator are available for selection by the output clock

selector. *See*, for example, FIG. 3 of Hashiguchi, which clearly illustrates that the only clock signals input to the output clock selector come from the serial clock generator. Although the clock signals are generated by the serial clock generator on the basis of a reference clock signal, the reference clock signal is not available to the output clock selector as an option for selection.

Since Mahajan in view of Hashiguchi does not teach or suggest Applicants' invention as recited in independent claim 23, the Applicants contend that claim 23 is patentable over Mahajan in view of Hashiguchi and, as such, fully satisfies the requirements of 35 U.S.C. §103.

III. Allowable Subject Matter

The Applicants thank the Examiner for the comments regarding the allowabilty of claim 18. In light of the above, the Applicants respectfully submit that claim 18 is allowable as it stands (*e.g.*, through it dependency from independent claim 14, which is believed to be allowable).

CONCLUSION

Thus, the Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §102 and 35 U.S.C. §103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring issuance of an adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Thomas George at 408-879-4682 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on September 2, 2009.
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